What is claimed is:

1. A semiconductor device comprising:

a drift layer of a first conductivity type;

a collector layer of a second conductivity type located on the drift layer;

a collector electrode located on the collector layer;

a base layer of the second conductivity type located in a region isolated from the collector layer on the drift layer;

a plurality of trenches formed at certain intervals to extend from the top surface of the base layer into the drift layer and thereby divide the base layer to main cell regions and dummy cell regions;

a first emitter layer of the first conductivity type selectively formed in the surface layer of the base layer in each main cell region to extend along adjacent one of the trenches;

gate electrodes formed in the trenches sandwiching each main cell region among said plurality of trenches via a gate insulating film;

an emitter electrode located over the base layer and the first emitter layer in each main cell region; and

a second emitter layer of the first conductivity type selectively formed so as to be scattered in the surface layer of the base layer in each dummy region and having a surface area smaller than that of the first emitter layer.

2. The semiconductor device according to claim 1,

wherein the drift layer of the main cell region has a carrier concentration profile having a peak on the side of the first emitter layer.

3. The semiconductor device according to claim 2,

wherein the drift layer of the main cell region forms a current path narrow enough to accumulate a carrier of the second conductivity type on and around the bottom of the

trenches when the device is turned on, and

wherein the second emitter layer forms a current path conducting a carrier of the second conductivity type to the emitter electrode by an amount not affecting the injection efficiency of the carrier of the first conductivity type from the emitter electrode to the drift layer when the device is turned on.

4. The semiconductor device according to claim 1,

wherein the second emitter layer is formed as isolated patterns in contact with the trenches opposed to each other via the base layer in each dummy cell region.

5. The semiconductor device according to claim 1,

wherein the second emitter layer is formed as island shaped patterns each having opposite ends in contact with the trenches opposed to each other via the base layer in each dummy cell region.

6. The semiconductor device according to claim 1 further comprising a via contact formed in contact with the second emitter layer to connect the base layer in the dummy cell region to the emitter electrode via the second emitter layer,

wherein resistance value of a floating resistor as a resistor between the base layer of the dummy cell region and the emitter electrode is adjusted by geometries of the second emitter layer and the via contact.

7. The semiconductor device according to claim 6,

wherein the resistance value of the floating resistor is 0.3 - 3 Ω when the applied voltage between the collector and the emitter is 600 V and the gate resistance is 51 Ω.

8. A semiconductor device comprising:

a drift layer of a first conductivity type;

a collector layer of a second conductivity type

located on the drift layer;

a collector electrode located on the collector layer;

a base layer of the second conductivity type located in a region isolated from the collector layer on the drift layer;

a plurality of trenches formed at certain intervals to extend from the top surface of the base layer into the drift layer and thereby divide the base layer to main cell regions and dummy cell regions;

a first emitter layer of the first conductivity type selectively formed in the surface layer of the base layer in each main cell region to extend along adjacent one of the trenches;

gate electrodes formed in the trenches sandwiching each main cell region among said plurality of trenches via a gate insulating film;

an emitter electrode located over the base layer and the first emitter layer in each main cell region; and

a second emitter layer selectively formed in the surface layer of the base layer in each dummy cell region,

wherein resistance value of a floating resistor as a resistance between the base layer of the dummy cell region and the emitter electrode is adjusted to be smaller than the resistance value causing rise of the gate-emitter voltage due to negative capacitance of the gate in a period to charge a gate charge between the gate and the collector by a voltage applied between the gate and the emitter when the device is turned on.

9. The semiconductor device according to claim 8,

wherein the drift layer of the main cell region has a carrier concentration profile having a peak on the side of the first emitter layer.

10. The semiconductor device according to claim 9,

wherein the drift layer of the main cell region forms

a current path narrow enough to accumulate a carrier of the second conductivity type on and around the bottom of the trenches when the device is turned on, and.

wherein the second emitter layer forms a current path conducting a carrier of the second conductivity type to the emitter electrode by an amount not affecting the injection efficiency of the carrier of the first conductivity type from the emitter electrode to the drift layer when the device is turned on.

11. The semiconductor device according to claim 8 further comprising a via contact formed in contact with the second emitter layer to connect the base layer in each dummy cell region to the emitter electrode via the second emitter layer,

wherein the resistance value of the floating resistor is adjusted by geometries of the second emitter layer and the via contact.

12. The semiconductor device according to claim 8,

wherein the second emitter layer is formed as isolated patterns in contact with the trenches opposed to each other via the base layer in each dummy cell region.

13. The semiconductor device according to claim 8,

wherein the second emitter layer is formed as island shaped patterns each having opposite ends in contact with the trenches opposed to each other via the base layer in each dummy cell region.

14. The semiconductor device according to claim 8,

wherein the resistance value of the floating resistor is 0.3 - 3 Ω when the applied voltage between the collector and the emitter is 600 V and the gate resistance is 51 Ω.